ON-CHIP MATCHING SI-MMIC FOR MOBILE COMMUNICATION TERMINAL APPLICATION

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ABSTRACT

Recent developments of BiCMOS Si-MMIC's for wireless communication applications are reviewed. Among these MMIC's, on-chip matching Si-MMIC's are suitable for use in compact transceivers. The use of coplanar waveguide (CPW) type spiral inductors is one of the solutions to achieve low loss matching circuits on a low resistive Si substrate used in standard BiCMOS process. An on-chip matching Si-MMIC front-end has been fabricated, in which CPW type spiral inductors are employed. The measured performance at 1.9GHz with low d.c. power consumption shows the possibility of application to mobile handset terminals. In addition, the feasibility to implement the system on-chip concept is discussed by referring to an IF / PLL IC fabricated in the same process.

I. INTRODUCTION

The performance of Si-MMIC's fabricated in BiCMOS process is approaching to commercial production level[1]-[6]. Since bipolar junction transistors (BJT's) have shown adequate RF performance with extremely low d.c.supply power to wireless communication handset terminals, they began to take the place of GaAs MESFET's in the field of receiving section which consists of discrete chip elements without any RF-IC.

There are two main features of Si-MMIC's fabricated in BiCMOS process. One is low production cost. By using conventional BiCMOS process[7], the chip cost per unit area is about 1/10 of that of GaAs MMIC's[8]. Second is the possibility to realize system on-chip concept. Since the device fabrication process of BiCMOS Si-MMIC's is compatible with that of IF / PLL / analog baseband(BB) IC's, all of these circuits can be integrated on single-chip without difficulties.

In section II, recent developments of BiCMOS Si-MMIC's for wireless application are reviewed. The states of art for low noise amplifier's (LNA's) NF and gain versus d.c. power consumption are presented. In section III, on-chip matching Si-MMIC is introduced. On-chip matching is one of the key concept to accomplish ultra compact mobile communication terminals. There, coplanar waveguide (CPW) type spiral inductors are introduced to achieve lower insertion loss on-chip matching circuits. By using CPW type spiral inductors, a 1.9GHz-band on-chip matching Si-MMIC front-end has been fabricated, which includes T/R MOSFET switch, two stage BJT LNA, and a down converter BJT mixer on single chip. The measured performance is also described. In section IV, the block diagram of RF / IF /PLL section for personal handy phone system (PHS) is presented and the possibility for obtaining single-chip transceiver IC is discussed, making reference to the developed BiCMOS IF / PLL IC[9] and the Si-MMIC front-end described in Section III. The measurement system and method are also presented.

II. RECENT DEVELOPMENTS OF BICMOS SI-MMIC FOR WIRELESS APPLICATION

From the point of view of LNA, recent studies are reviewed. Figure 1 shows NF versus d.c. power consumption and Fig. 2 shows the gain versus the d.c. power consumption. In both figures, the plots are categorized into three, i.e. external matching BJT based Si-MMIC's [1]-[4], on-chip matching BJT based Si-MMIC's[5]-[6] and MOSFET based Si-MMIC's [1][10]. The performance of both external and on-chip matching BJT based Si-MMIC's is approaching to competitive level with commercial GaAs-MMIC's for mobile terminal use[11]. The development of MOSFET based Si-MMIC's stands at the starting point and it will take time to catch up with the BJT based Si-MMIC's.

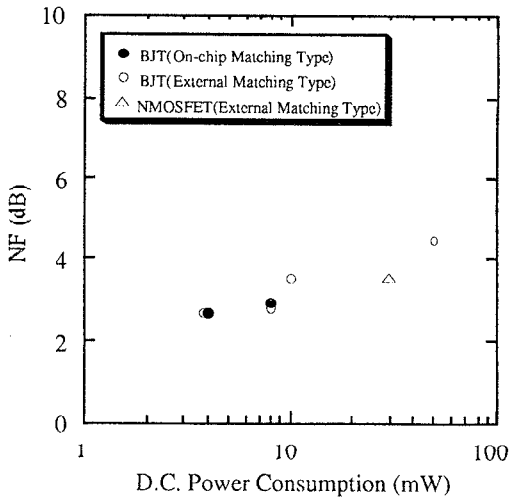

Fig.1 NF versus d.c. power consumption of BiCMOS / CMOS LNA. (Performance of BJT based is at 1.9GHz, and that of NMOSFET based is at 1.5GHz)

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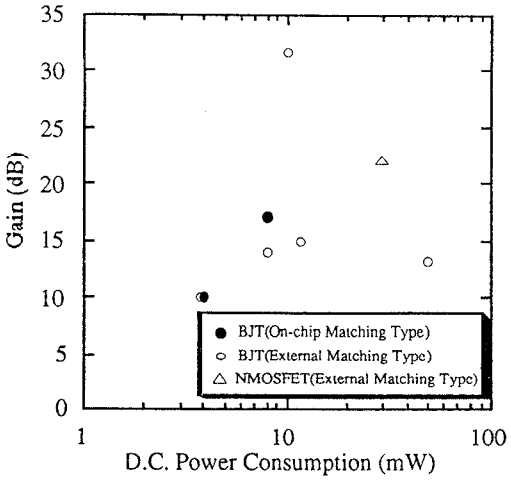


Fig.2 Gain versus d.c. power consumption of BiCMOS / CMOS LNA. (Performance of BJT based is at 1.9GHz, and that of NMOSFET based is at 1.5GHz)

III. ON-CHIP MATCHING SI-MMIC

On-chip matching circuits are strongly desired to realize ultra compact and low production cost handset terminals. Since the standard BiCMOS process uses relatively low resistive Si substrate (about 10 Ωcm), the loss of on-chip matching circuits, especially that of spiral inductors is quite high due to the dielectric loss of Si substrate at microwave frequency range. CPW type spiral inductor is capable of reducing its attenuation in comparison with conventional microstrip line (MS) type one. Table I shows the extracted equivalent circuit parameters and the attenuation of CPW and MS type four-turn spiral inductors at 1.9GHz. In order to extract the parameters, the equivalent circuits, shown in Fig. 3, are used. The reduction of Rp in the case of CPW indicates reduction effect on the dielectric loss of the substrate.

Figure 4 shows a schematic diagram of the IC front-end. This IC consists of MOSFET T/R switch[12], two-stage BJT LNA, and down converter BJT mixer. T/R switch: Enhancement mode N type MOSFET's are used, and they are switched by the gate control voltage of 0V (OFF state) / 3V (ON state). In order to achieve higher isolation in OFF state, the FET's are series-shunt connected. LNA: The input port is NF matched, and the output port is gain matched to 50 Ω by using CPW type spiral inductors. Mixer: The BJT's of the same emitter size are connected in series. RF and LO ports are internally matched to 50 Ω, whereas IF port requires external matching circuits.

Figure 5 shows a photograph of fabricated RF front-end Si-MMIC. The chip size is 2mm×2mm, and the IC is fabricated in standard 0.8μm BiCMOS process[7]. The aluminum metal surrounding strip line and transistors is the ground metal of CPW.

Table 1 Extracted equivalent circuits parameters and attenuation of CPW and MS type four-turn spiral inductors. (Outer size: 300μm × 300μm, conductor thickness: 3.5μm, stripline width: 11μm, line space: 10μm)

Type	CPW	MS
Ls (nH)	4.2	4.2
Cp (pF)	0.4	0.46
Rs (Ω)	4.6	3.3
Rp (Ω)	136	246
Attenuation (dB)	1.5	1.8

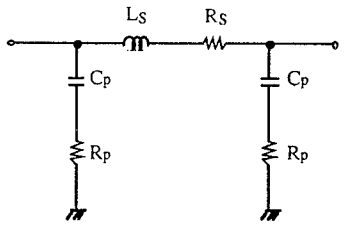


Fig.3 Equivalent circuit of spiral inductors fabricated on low resistive Si substrate. Rs represents the conductor loss, Rp represents the dielectric loss of the spiral inductor, Ls represents the inductance component of the spiral inductor and Cp represents the stripline - substrate capacitance.

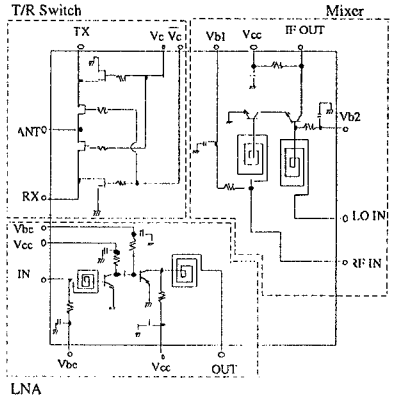


Fig.4 Schematic diagram of on-chip matching Si-MMIC front-end.

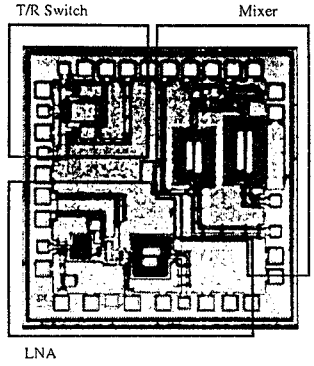


Fig.5 Photograph of fabricated Si-MMIC front-end.(Chip size: 2mmx 2mm)

Figure 6 shows the small signal characteristics of the T/R switch. Figure 7 shows the transfer characteristics of the switch at 1.9GHz. Figure 8 shows the frequency dependence of gain and NF of the two-stage BJT LNA. The bias condition is Vcc=2V, Ice(LNA total)=4mA. The gain is 17.1dB and the NF is 2.9dB at 1.9GHz. Figure 9 shows the frequency

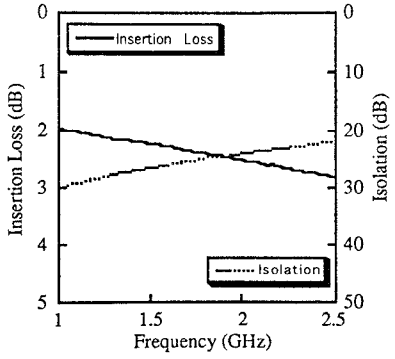


Fig.6 Small signal characteristics of T/R MOSFET switch. (Control voltage of 0 / 3V)

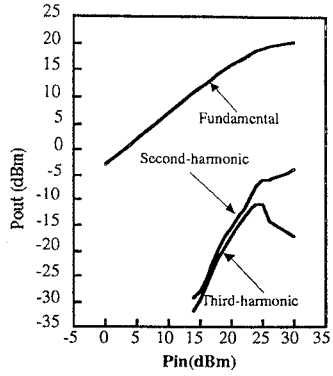


Fig.7 Transfer characteristics of T/R MOSFET switch measured at 1.9GHz. The control voltage is 0V(off state) and 3V (on state).

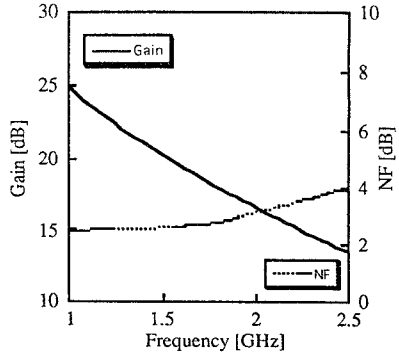


Fig.8 Frequency dependence of gain and NF of two-stage BJT LNA. (2V, 4mA)

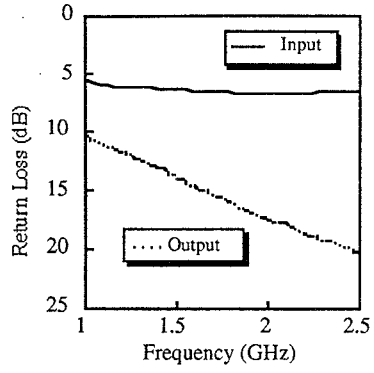


Fig.9 Frequency dependence of return loss of two-stage BJT LNA. (2V,4mA)

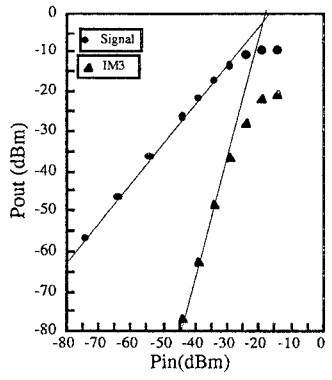


Fig.10 Two-tone transfer characteristics of two-stage BJT LNA. (2V,4mA)

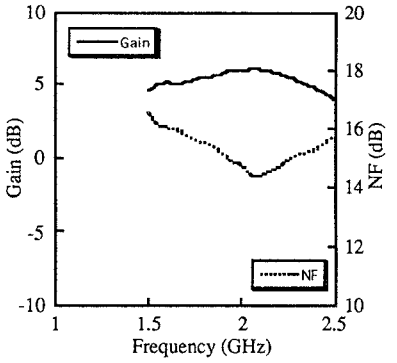


Fig.11 Frequency dependence of conversion gain and NF of BJT mixer. (2V, 1.7mA)

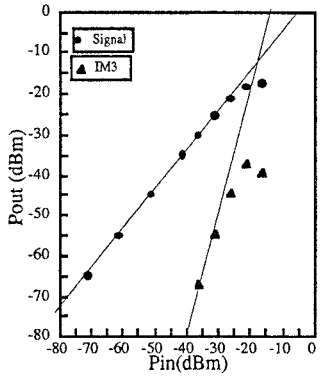
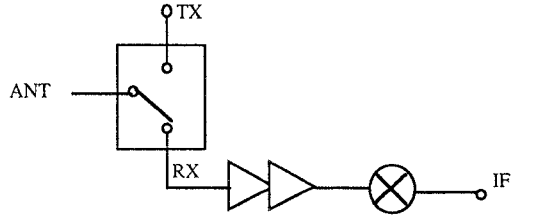


Fig.12 Two-tone transfer characteristics of BJT mixer. (2V, 1.7mA)



	SW	LNA	MIX	Total
Gain (dB)	-2.5	17.1	5.9	20.6
NF (dB)		2.9	15.0 (SSB)	6.6
P_{DC} (mW)	0	8.0	3.4	11.4

Fig.13 Block diagram and performance of Si-MMIC front-end.

dependence of return loss of the LNA. Figure 10 shows the two-tone transfer characteristics of the LNA at 1.9GHz. Figure 11 shows the frequency dependence of conversion gain and NF of BJT mixer. Figure 12 shows the two-tone transfer characteristics of the LNA at 1.9GHz. By using this IC, the RF front-end having NF of 6.6dB, including the loss of the T/R switch, can be realized at 1.9GHz with 11.4mW d.c. power consumption as shown in Fig.13.

IV. FEASIBILITY OF IMPLEMENTING SINGLE-CHIP TRANSCEIVER IC

Since BiCMOS process is widely used for IF / PLL / analog BB IC's, the BiCMOS RF-IC's are capable of being merged into the same chip. Figure 14 shows a block diagram of RF / IF /PLL section of PHS handset.

By combining two BiCMOS Si-IC's, Si-MMIC mentioned in

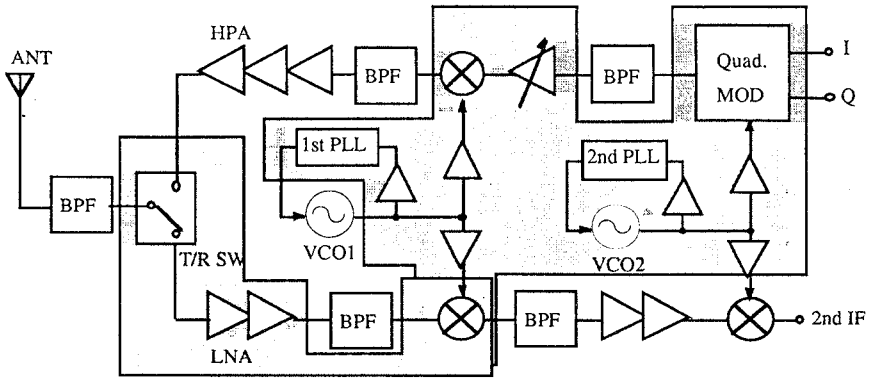


Fig.14 Block diagram of RF / IF /PLL section of PHS handset

section III and IF / PLL IC (M64820FP, Mitsubishi)[9], almost all active / control circuits except an HPA, VCO1 for 1st local, and IF amplifier for receiver can be integrated on single Si-chip.

V. CONCLUSION

In recent years, the performance of BiCMOS Si-MMIC's is approaching to commercial product level for wireless application. Among these IC's, on-chip matching IC has an attractive feature to achieve ultra compact handset. A 1.9GHz-band on-chip matching Si-MMIC front-end has been introduced. The IC consists of a T/R switch, a two-stage LNA, and a down converter mixer. The fabricated Si-MMIC operates with only 11.4mW supplied d.c. power and the measured performance indicates the feasibility of application to mobile handset terminals. By integrating with IF / PLL IC fabricated in the same process, it will be possible to realize a single-chip transceiver IC.

REFERENCES

[1] M. Madihian,"Low Voltage Broadband BiCMOS MMICs for Low-Cost High-Speed Wireless Networks Applications," in Proc. 1996 Microwave and Millimeterwave Monolithic Circuits Symposium, pp.57-60, 1996.

[2] C. Takahashi, R. Fujimoto, S. Arai, T. Itakura, T. Ueno, H. Tsutsumi, H. Tanimoto, S. Watanabe and K. Hirakawa, "A 1.9GHz Si Direct Conversion Receiver for QPSK Modulation Systems", 1995 IEEE ISSCC Digest of Technical Papers, pp.138-139, 1995.
1996.

[3] J. R. Long, M. A. Copeland, P. Schvan and R.A. Hadaway,"A Low-Voltage Silicon Bipolar RF Front-End for PCN Receiver Applications", 1995 IEEE ISSCC Digest of Technical Paper, pp.140-141,1996.

[4] W. Titus, M. Shifrin, V. Aparin and B. Bedard, "A Silicon BiCMOS Transceiver Front-End MMIC Covering 900 and 1900MHz Applications", in Proc. 1996 Microwave and Millimeterwave Monolithic Circuits Symposium, pp.73-76, [5] N.Suematsu, M.Ono, H.Sato, S.Kubo,Y.Iyama, O.Ishida,"A L-Band Internally matched Si-MMIC Low Noise Amplifier", 1996 IEEE MTT-S Digest, pp.1225-1228, 1996.

[6] N.Suematsu, M.Ono, H.Sato, S.Kubo,Y.Iyama, O.Ishida, "L-Band Internally Matched Front-End Si-MMIC", in Proc. 26th. European Microwave Conference, pp.37-41, 1996.

[7] T.Ikeda, T. Nakanishi, S. Kubo, H. Jouba and M. Yamawaki, "A high performance BiCMOS with Novel Self-Aligned Vertical PNP Transistors", in Proc. IEEE 1994 Bipolar/BiCMOS Circuits and Technology Meeting, pp.238-241, 1994.

[8] M.Golio, "HF Devices for Mobile Communications", 1995 IEEE Int. Topical Meeting on Normadic Microwave Tech. and Tech. for Mobile Commun. and Detection, pp.3-9, 1995.

[9] H.Sato, K.Kashiwagi, K.Niwano, T.Iga, T Ikeda, K.Mashiko,"A 1.9GHz Single-Chip IF Transceiver for Digital Cordless Phones", 1996 IEEE ISSCC Digest of Technical Papers, pp.342-343, 1996.

[10] D. K. Shaeffer and T. H. Lee," A 1.5V, 1.5GHz CMOS Low Noise Amplifiers," 1996 Symposium on VLSI Circuits Digest of Technical Papers, pp.32-33, 1996.

[11] N.Suematsu, M. Shimozawa, K. Mori, Y. Nakashima, K. Maemura, O.Ishida, "Low Power Consumption RF IC's for Japanese Mobile Handset Terminals", Proc. of 1995 IEEE Int. Topical Meeting on Normadic Microwave Tech. and Tech. for Mobile Commun. and Detection, pp.39-42, 1995.

[12] Y. Iyama, N. Suematsu, T. Shigematsu, T. Moriwaki and T.Ikeda, "L-Band SPDT Switch Using Si-MOSFET", IEICE Trans. Electron, vol.E79-C, pp.71-76, 1996.